PROJECT

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INTERIM RESEARCH REPORT NO. 16A

for

HIGH-SPEED DATA PROCESSOR SYSTEM RESEARCH

Project LIGHTNING

This report covers the period of
August 31, 1962 to November 30, 1962

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Prepared by
Engineering Department
Electronic Data Processing Division
Industrial Electronic Products
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Camden, New Jersey

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Chapter 1. GENERAL

1-1. INTRODUCTION AND INTERPRETIVE SUMMARY

During this quarter the combined Logic and Memory Subsystems were operated in life-test fashion in an effort to define the problems associated with reliable performance.

A. LOGIC SUBSYSTEM

The reliability of the Logic Subsystem is at present better than that of the Memory Subsystem primarily because the models used in performing the worst-case designs were more accurately predictable, since the signals and noises involved were more of a standard nature. As a result the information obtained from this portion of the work is very meaningful in proving the design predictions. To date, there have been an accumulation of approximately 1,500 hours of running time upon this subsystem and several important observations can be made at this point.

In agreement with the prediction of our device life test, the number of failures of tunneling devices classified as drift have been very small. While there have been a number of catastrophic failures, it is believed that this is a result of the fact that the units were built with several different fabrication techniques. A large number, having been built with very early techniques, did not have the built-in reliability characteristics of the present units. Gradually however, the more marginal units are being replaced and, as a result, the present reliability is greatly improved over that experienced in the early hours of operation. For example, in the last 285 hours of operation only one tunneling device failed. As a result of the experience gained, we have great confidence in our ability to generate and distribute the d-c power required to operate these circuits. One of the earlier fears was born of the fact that d-c must be generated and distributed in the mv range as opposed to the several volt level of transistor circuits. We were concerned both with regulation in the distribution lines and drift of the voltages. It appears that both of these fears were unfounded. While many of the fabrication problems have at least tentative satisfactory solutions, a number of weak areas have been defined. We have learned, for example, a considerable amount about soldering, both of devices and components, and this has been demonstrated by the fact that only one solder failure was evident during the entire quarter. We have also profited from our experience with solid-jacket coax.

B. MEMORY SUBSYSTEM

The total number of hours accumulated upon the Memory Subsystem is appreciably in excess of 1,300. While the reliability encountered in this subsystem is not on a

par with that evident in the Logic Subsystem, we have, nevertheless, defined much of the problems and reliable operating time is being increased week by week. We have learned much about the problems associated with the use of connectors for the relatively small wafers. Although the logic wafer connectors had insufficient contact pressure, we have discovered ways of building up the wafer pads with gold wires so that reliable operation could be obtained. We have found that our basic assumption on the designs of the GaAs circuit (which followed the rule of operating in the forward-current region equal to or less than .8 of the valley capacity) is valid. Although the catastrophic failure of the GaAs units at the present time has been somewhat greater than that of the Ge units, drift failures have been about equal. We have learned that attaching tunneling devices by means of epoxy mounting is adequate for high impedance circuits. Our memory plane reliability was much improved when we covered each of the memory cell electrical connections with conductive epoxy.

Total hours of combined operation of the Memory and Logic Subsystems have been relatively small because of such factors as insufficient d-c supply stability (ordinary lab supplies were used) and noise pick up. It is felt that the noise problem requires a complete reconstruction in which the total memory and all of its peripheral circuits are built on a unified chassis as opposed to the present scheme of several different parts interconnected with coaxial cable.

Reliability, however, is improving continuously and we are satisfied that the systematic timing is adequately proved since the subsystem performs all of the functions at the speed for which it was designed.

Chapter 2. COMBINATION

I. PERSONNEL

The following personnel contributed to this phase of the project during the sixteenth quarter:

R. H. Bergman
F. Borgini
J. Schopp

II. DISCUSSION

A. GENERAL

During this quarter effort ensued on the Logic and Memory Subsystems for maintaining reliable integrated operation and to obtain reliability data. The first part of this chapter deals largely with the Memory Subsystem, including all the equipment on the memory table. The second part contains the reliability information thus far obtained on the logic circuitry.

The memory table contains the memory stack with its word drivers, sense amplifiers and digit drivers, the decoder, memory address counter, read-write register (R-WR), the inhibit sense amplifier (ISA), the timing generator, the counter-decoder console, a small memory console, and power supplies for all the above. For accessibility and convenience, the lower planes of the memory were not operated during most of this phase.

Integrated operation involves circulating information between logic and memory, incrementing by one the contents of a word after each transfer from memory and changing to the next word when the A Register is filled. At all times parity is checked and any parity errors which occur are counted.

Therefore, the system runs continuously, exercising every memory location and logic circuit. Most of these circuits operate at an irregular repetition rate, (as they would in a full-size machine) and all are self checked.

At the beginning of this phase, this mode of operation would not work at all; in fact, it would not run without errors on any one word. Therefore, the Logic and Memory Subsystems were run separately for the first few weeks.

Next, the grounds were checked and modified resulting in removal of the circulating 60-cycle currents. This made the system more noise immune. Several sources of noise (such as defective fans) were found, corrected and removed. The bias ranges of the sense amplifiers were increased by replacing some of the tunnel rectifiers in the memory with units having lower capacity and by replacing some of the preamp diodes with faster ones. Other biases were checked and some of the power supplies were stabilized (drift reduced from +1.5% to a few tenths of one percent).

Integrated operation of both subsystems was again attempted at SKL and stepping rates until all the words could be run while incrementing bits (although not changing words). About this time it became apparent that the Memory Subsystem was plagued with an inordinate number of failures and breakdowns, some of which were so subtle that everything seemed to operate satisfactorily until word changing was attempted.

Thus, it was decided to keep a record of all repairs, changes, etc, before consistent integrated operation was achieved. Table 2-1 is a summation of this record covering the two-month period from September 25 to November 26 (45 working days), from 974 hours to 1,334 total hours of memory operation exclusive of logic.

TABLE 2-1
SUMMATION OF MEMORY REPAIRS (9/25-11/26)

Action	No. of Times	No. Wafers Affected
Restoration of Contact by Wafer Manipulation	48	20
Wafer Removal	41	40
Check and Clean	13	13
Apply Gold to Contacts	8	8
Diode Replacement	11	10
Diode Soldering	6	6
Other	3	3
Soldering Repairs	18	
Loose Diodes	11	
Other	7	
Bias Adjustment (To restore operation etc.)	33	
Apply Gold to Wafer Signal Pads		10
Cable Repairs	8	
Microdot	3	
Subminax	5	
Diodes Replaced*	21 Diodes	

*Prime Failures only - Failure due to other diode failures or damage due to servicing not counted

TABLE 2-1 (Continued)
SUMMATION OF MEMORY REPAIRS (9 25-11 '26)

Action	No. of Times
Design Changes	7
Delays	2
ISA Shunt Resistors	5
Applied Conductive Epoxy to Diodes in Holders	101 Diodes
Replaced Other Components	2 - 81.6 Ω Resistors
Power Lines	9
Tighten Screws	4
Repair Opens or Shorts	4
Repair Split Lines	1
Timing Gen. Adj or Repair	7
Miscellaneous Repairs	14

B. DISCUSSION OF PROBLEMS

By far the largest number of failures was due to the wafers themselves as evidenced by the large number that had to be manipulated, wiggled or removed to restore contact. This problem stems from the decision to use wafers that were already built and designed for soldering connections in a newly developed pluggable frame. This problem does not exist in the earlier built Logic Subsystem; however, repairs are extremely difficult and can only be done by a few highly skilled people. Thus, removable wafers are highly desirable, provided they can be made more reliable. A complete investigation to determine precisely where the failures are occurring (power or signal contacts, etc.) has not yet been made because of the difficulty of the problem, lack of time, and the urgency of other problems preventing consistent operation. However, there is evidence showing that most, but not all, failures occur at the signal contacts. Subsequent designs include gold to gold contacts, higher contact pressures, and better control of the factors which influence the contact pressure tolerance. Gold has been applied to the signal contacts of 10 wafers, thus the future record of these wafers may shed some light on the problem.

Table 2-1 shows that the biases were adjusted a large number of times to restore operation. However, a recent check of all the bias ranges showed that most are far less critical than previously believed and only one, the write drive bias, is at present less than the stability of its supply. (See bias range in Table 2-2).

TABLE 2-2
OPERATING POWER SUPPLY BIAS RANGE

Supply	Min. Voltage	Max. Voltage
Memory Cell	2.17	2.30
XSMD	5.94	6.23
CLXS	10.4	12.0
D.D.II	9.17	9.57
D.D.I	6.33	6.66
D.D.III	.883	1.5
SAIB (preamp)	.908	.943
SAIA	.947	.972
CLISA	11.7	13.5
YSMD	12.5	13.0
SAII	6.26	7.24
SAIII	1.78	7.35
RD.-I	4.25	5.37
WD-SW	3.94	4.55
RD-II	13.0	13.9
WR-II	10.6	10.7
-90 MV	.051	.137
+90 MV	.086	.096
+6 I Volts	5.87	6.05
+6 II Volts	5.94	6.65
-6 Volts	5.93	6.37

Thus, when bias adjustment restores operation, it usually is compensating for some other defect. This phenomena has led to the use of bias adjustment as a very useful diagnostic tool, where there are not too many circuits of different types on one supply.

Of the 17 soldering repairs, nine were for loose diodes. However, there are 1501 soldered diodes in the Memory Subsystem and possibly several of these were loosened by checking for other troubles such as contact failures. The other eight were easy to repair but not always easy to find.

The shields of two signal cables to the ISA frame appeared well soldered but were evidently only making physical contact since their installation. As oxidation increased, operational failure and intermittency also increased. Until this problem was finally tracked down, much time was lost due to fruitless and frustrating searches and repairs.

Of the eight cable connector repairs, three were microdot. Since there were only 25 microdot connections involved this is a high percentage; thus this type of cable, though handy for removal, should be avoided for this service. Of the hundreds of screw type (subminax) connectors, only five had to be repaired and some of these could have been prevented if they had been protected from extraordinary stress. Some failures were due to loose cables (not listed), however many of these connections have been opened many times for the purpose of check-out, diagnosis, checking and changing delays. There are 47 connections to the heavy low-impedance power lines using 2-56 brass screws. These had to be checked and/or tightened 4 times during the two month period. The d-c voltages were normal at all pertinent points yet error-free operation was restored when these screws were tightened. A 2-56 brass screw may not be strong enough here to maintain sufficient contact pressure.

Seven failures were due to diminishing output of the timing generator. This has been isolated to the transmitter and is believed to be due to an intermittent in the driver stage. As of now it has not been located nor repaired.

There is a total of 1,708 tunnel diodes now being operated. Twenty-one of these diodes failed and were replaced during the two-month (360 hours) period. Most of these had at least 1,000 hours of service. These were all due to prime failures and do not include diodes that failed because other diodes failed nor diodes accidently damaged (such as shorting with a scope probe or over-heating with a soldering iron while making adjacent repairs). Table 2-3 is a breakdown of these failures.

This table shows that the failure rate for all types of diodes in the Memory Subsystem was 3.43% per 1,000 hours. This compares unfavorably with the Logic Subsystem which had a failure rate over the same period (Sept. 25 to Nov. 26) of .06% and has had only one of its 2,715 diodes replaced in the past 419 hours of operation. The reason for this discrepancy is not known; however, it may be due to:

(1) The Logic Subsystem data includes less of the "debugging" period.

(2) Diodes were replaced during this period which should have been replaced sooner.

(3) Diodes may have been unwittingly damaged while making some of the numerous other repairs or checks.

(4) The poor contacts may have introduced damaging transients.

Of the 697 rod resistors in the Memory Subsystem, two 81.6-ohm resistors had to be replaced during this period. This represents a failure rate of .8% per 1,000 hours for all rod resistors and 15% per 1,000 hours for 81.6-ohm rod resistors. These resistors increased about 5% in value.

TABLE 2-3
MEMORY SUBSYSTEM PRIME DIODE FAILURES
(1,000 HRS. OF OPERATION)

Diode Type	No. Used	Catastrophic No. %/1000 hrs.	Degenerative No. %/1000 hrs.	Total No. %/1000 hrs.
GaAs TD	68	1 - 4.08% Suspicious - 1 (intermittent)	2 - 8.16% High E_p - 2	3 - 12.25%
GaAs TR	40	0	0	0 - 0.0%
Ge TD	403	3 - 2.06% Open - 3	3 - 2.06% High valley - 1 High E_f - 1 Low peak - 1	6 - 4.12%
Ge Clamps	431	2 - 1.29% Shorted - 2	4 - 2.58% High E_R - 4	6 - 3.87%
Ge OR	549	4 - 2.03% Open - 3 Shorted - 1	2 - 1.01% High E_R - 2	6 - 3.04%
Ge AND	217	0 10 - 1.63%	0 11 - 1.80%	0 21 - 3.43%

C. MODES OF OPERATION

When the Memory and Logic Subsystems operate together, several modes of operation are possible depending on the contents of the memory at the start. One possible mode is where all the words are on about the same amount of time (as judged by the lights on the decoder console). In another mode, the "odd" mode, the odd words are on most of the time. The even mode, and perhaps other modes are also possible. The mode of operation can be changed by writing into the memory from one of the consoles. A total of only about 16 hours of this type operation has been achieved thus far with a maximum error-free period of 40 minutes, which was accomplished recently. However, the ratio of proper operating time to total operating time is increasing and thus it is hoped to achieve satisfactory, consistent operation in the near future.

D. OPERATION OF LOGIC SUBSYSTEM

During this quarter, the Logic Subsystem clocked a total of 625 operating hours, raising the net to 1,540 hours of operation. There were 13 catastrophic failures during this period. At 963 hours, this subsystem was placed on 16-hours per day operation and data were recorded each day.

The catastrophic failures of the Logic Subsystem are listed in order in Table 2-4. The failures include 5 tunnel diodes, 3 clamps, 2 rectifiers, 1 resistor, 1 solder connection and 1 coax cable. There have been only 2 failures in the last 380 hours. The Logic Subsystem contains 2,715 tunnel diodes and tunnel rectifiers.

During the last eight hours of the 16 hours of daily operation, this subsystem is observed in order to record all errors occurring during operation. An error differs from a failure in the respect that the subsystem need not be shut down and repaired. Data are also recorded as was proposed earlier.

The graphs of Figures 2-1, 2-2 and 2-3 indicate the variation in the +90 mv, +6.0 v, and -6.0 v power supplies of the Logic Subsystem, up to the point where the system produces a malfunction. These variations were taken while the subsystem was running in its normal mode of operation. ($\overline{\text{INT}}$, $\overline{\text{STEP}}$, REP.).

Figure 2-4 shows the time it takes to complete commands from the control logic vs. hours of operation. There is no indication of any change in these times. The variations are due to measurement discrepancies. These curves are typical of other measurements made; for instance, the period of the control program vs. hours of operation; and the transit time through a typical signal path vs. hours of operation, which also show no distinct changes.

All errors made by the subsystem were recorded during the second half of the 16-hour daily periods. There is no indication of malfunctions due to noise sensitivity. All malfunctions were due to intermittent conditions which eventually resulted in a major repair. Figure 2-5 shows a curve of the number of errors made versus a 7-hour period of observation. The errors were detected individually by removing the PEO in the Logic Subsystem, thereby stopping the system for each malfunction.

High repetition rate tests have been performed in the A register to demonstrate shifting and counting. The maximum input repetition rate for counting is 195 mc and for the shifting function it is approximately 125 mc. There has been little variation from these figures.

A record has been kept on a group of d-c bias points in the system. There is no variation at all in these bias values, indicating the drift in the components is not significant.

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TABLE 2-4
SUMMARY OF FAILURES AND REPAIRS IN LOGIC SUBSYSTEM

Hours of Operation	Location and Type of Failure	Repair Made
820	X-Reg OR 6-p 140-ohm resistor out of spec (2nd stage bias low)	Replaced resistor
828	CONTROL OR 3-T input rectifier diode open	Replaced rectifier diode
837	CONTROL AND 4-S 35-ma TD open (3rd stage)	Replaced 35-ma TD
866	A-Reg Bistable 11-K 25-ma TD out of spec in inverter	Replaced 25-ma TD
895	CONTROL Bistable 7-G clamp diode open in inverter	Replaced clamp diode
1,017	CONTROL Bistable 8-F clamp diode out of spec in inverter	Replaced clamp diode
1,026	PARITY CHECKER Delay 4-V output rectifier open	Replaced rectifier diode
1,033	X-Reg Bistable 11-P current biasing resistor unsoldered in set amplifier	Resolder resistor
1,041	X-Reg Bistable 4-P 24.5-ma TD out of spec in set amplifier	Replaced 24.5-ma TD
1,103	CONTROL delay 10-F 50-ma TD open in inverter	Replaced 50-ma TD
1,163	X-Reg Bistable 13-M AND diode open in inverter	Replaced AND diode
1,456	A-Reg Bistable 12-E 25-ma TD out of spec in inverter	Replaced 25-ma TD
1,472	X-Reg Signal cable from wafer 3M-8N has outer conductor cracked	Soldered over crack in shield

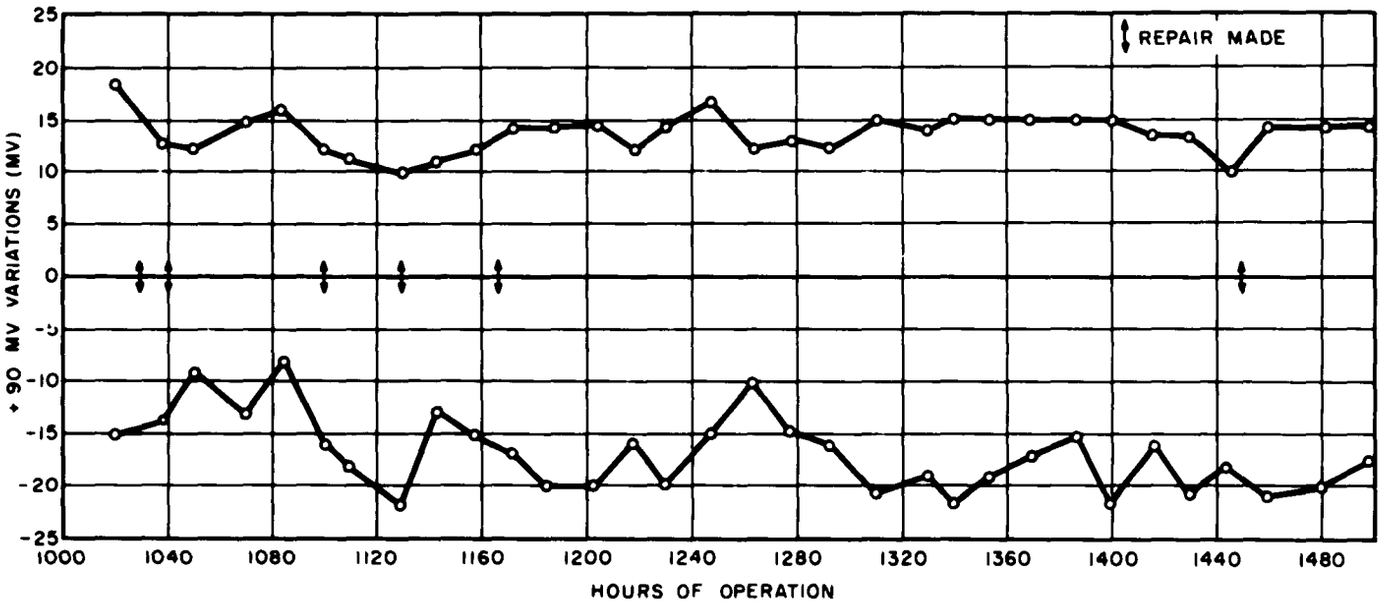

Figure 2-1. +90MV Variation of Logic Subsystem vs. Hours of Operation in its Normal Operating Mode

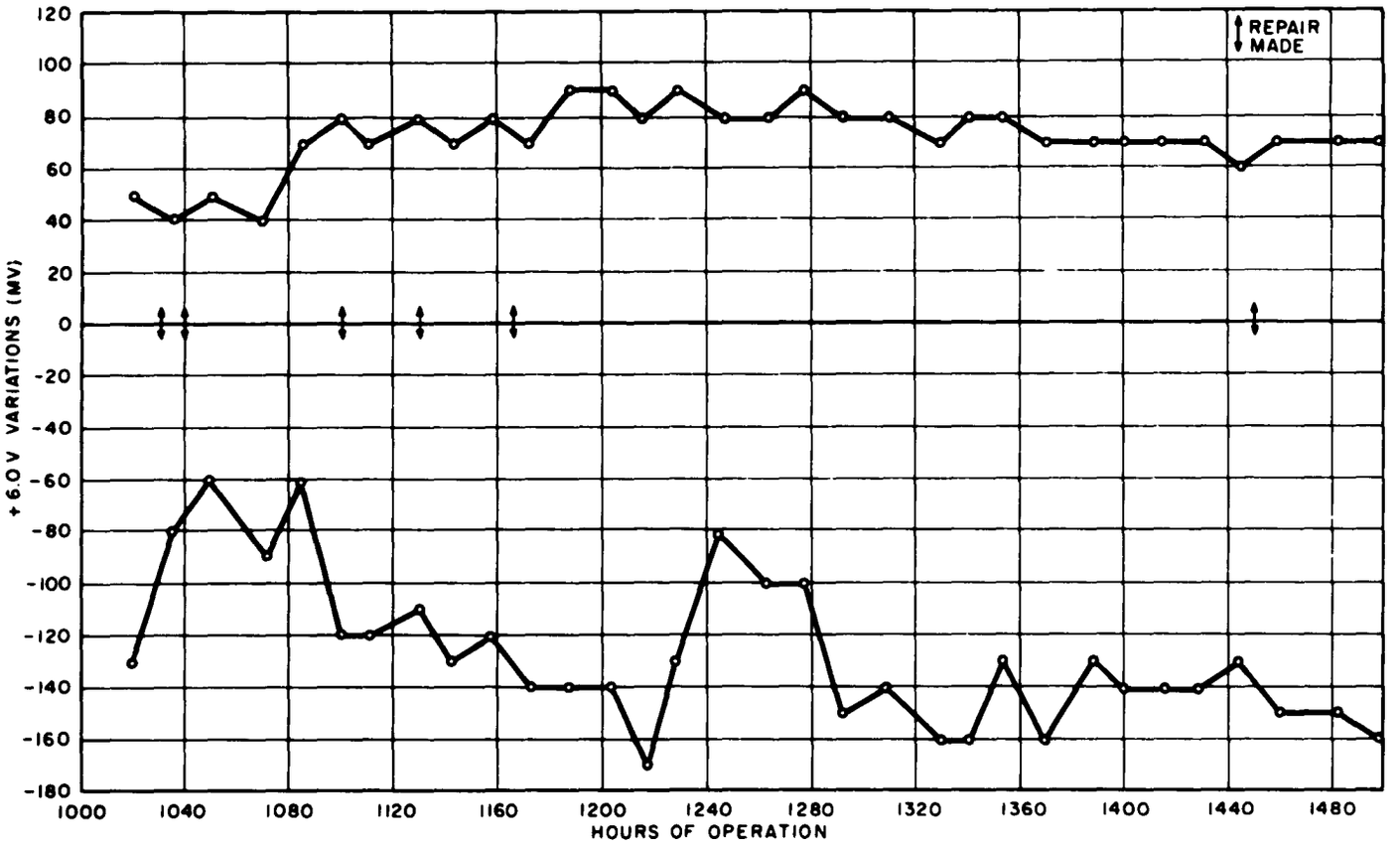

Figure 2-2. +6.0V Variation of Logic Subsystem vs. Hours of Operation in its Normal Operating Mode

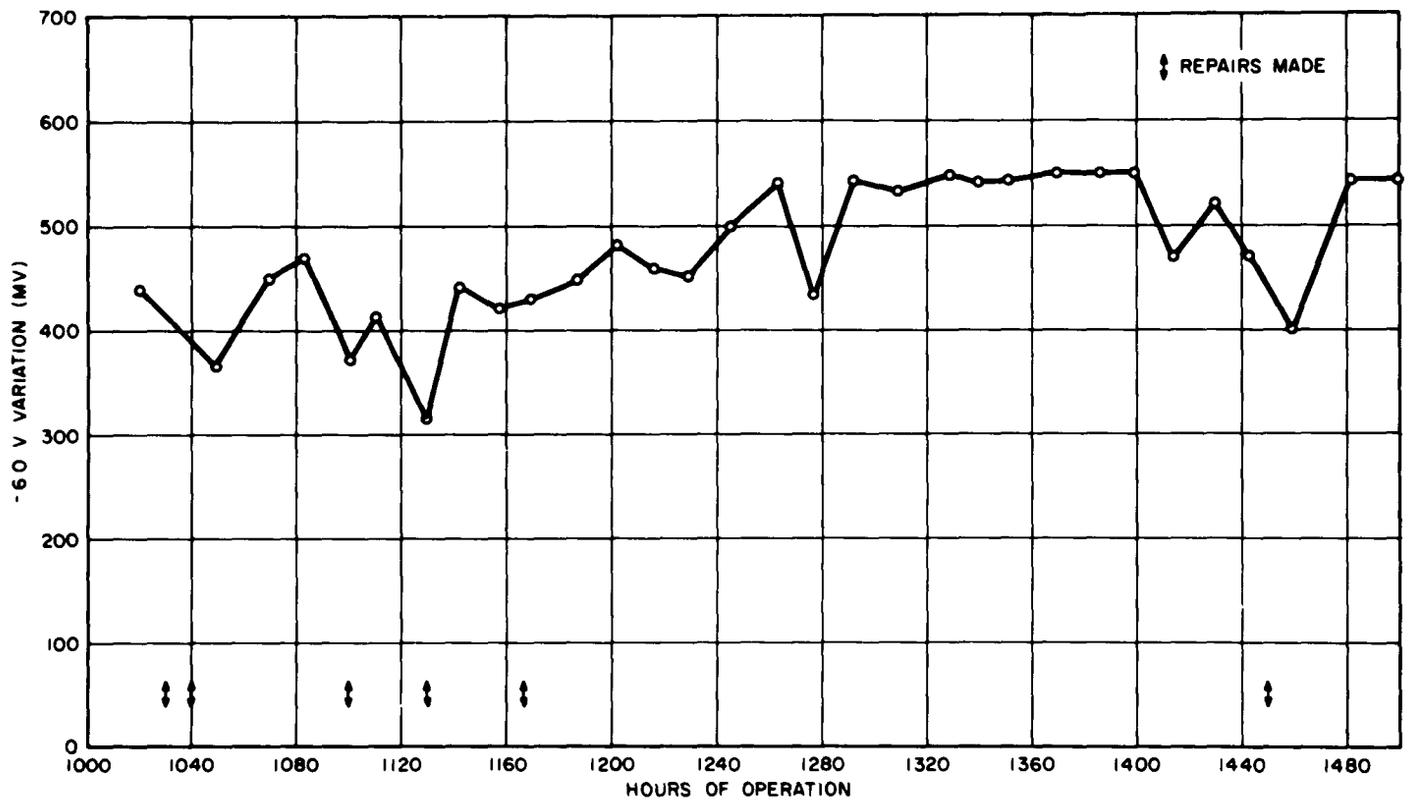

Figure 2-3. —6.0V Variation of Logic Subsystem vs. Hours of Operation in its Normal Operating Mode

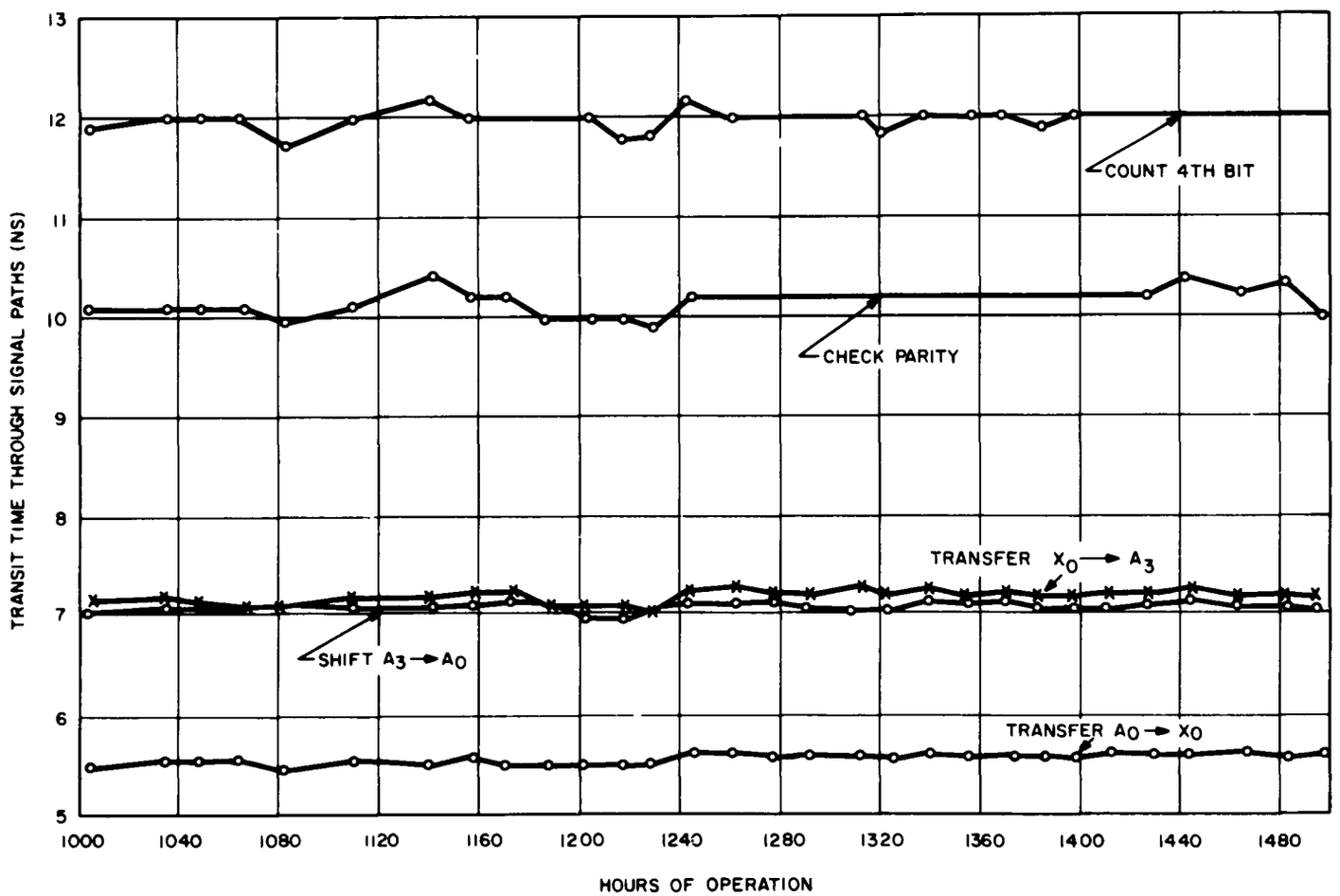

Figure 2-4. Plot of Time to Complete Control Commands vs. Hours of Operation in the Logic Subsystem at Nominal Voltages

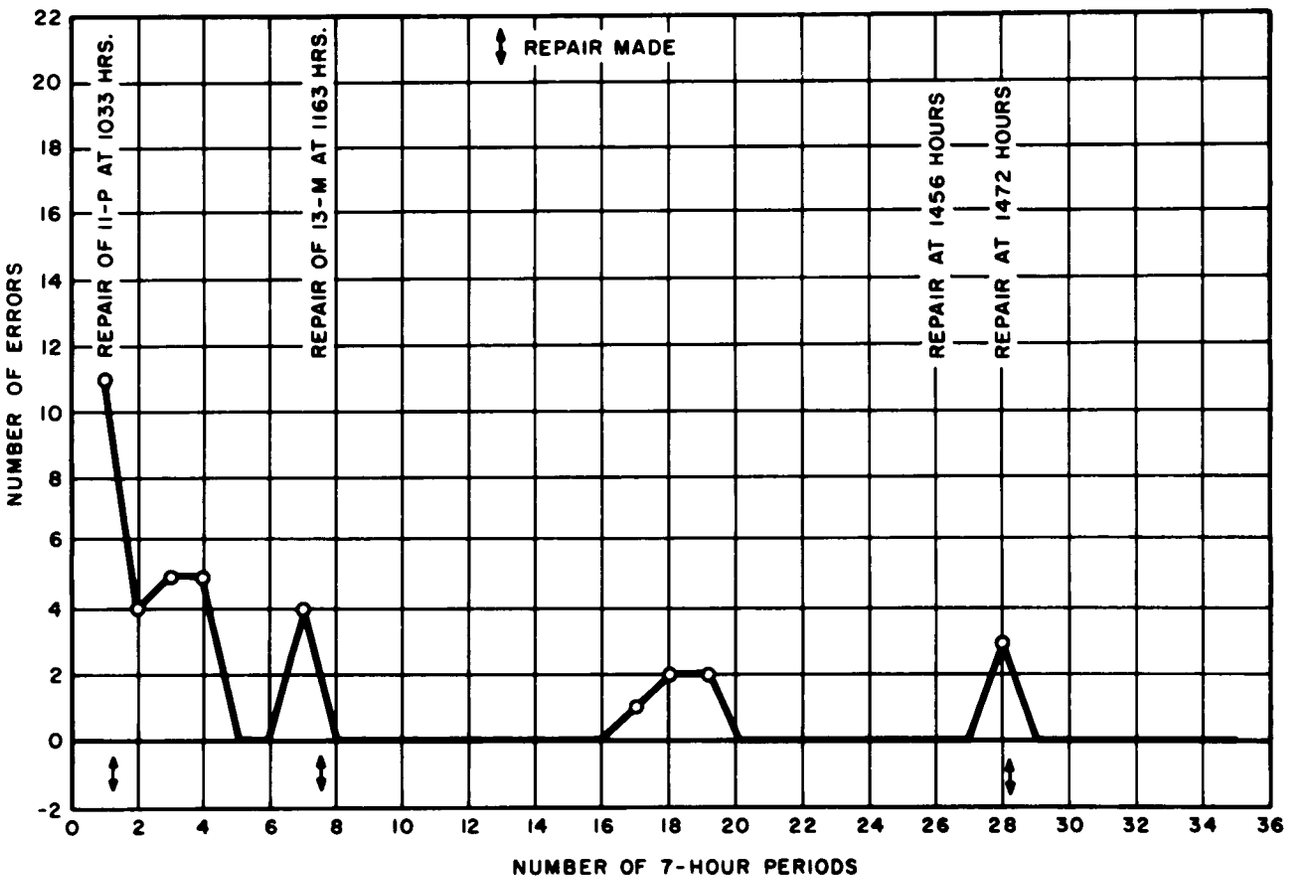

Figure 2-5. Number of Errors vs. Number of 7-Hour Periods of Logic Subsystem Operation

III. PROGRAM FOR NEXT INTERVAL

Operation of the Combined Subsystem will continue throughout the quarter and a final report will be issued.